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10/708,948	04/02/2004	Andrew Chang	MTKI0071USA	2947

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
SINGH, HIRDEPAL	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
04/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.	Applicant(s)	
	10/708,948	CHANG ET AL.	
	Examiner	Art Unit	
	HIRDEPAL SINGH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10-17* is/are rejected.

7)☒ Claim(s) *3-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on January 31, 2008. Claims 1-17 are pending and have been considered below.

Response to Arguments

2. Amendment has properly addressed and corrected the informalities in the specification. Therefore, the objection to the specification is withdrawn.

3. Applicant's arguments filed January 31, 2008 have been fully considered but they are not persuasive.

4. Applicant's compliment, that "... cited references are reasonably combined..." on page 11, lines 20-22 of the amendment, is greatly appreciated by the examiner.

5. Applicant argues "...claim 1 of the applicant's disclosure includes the limitations: a comparing device...for comparing the input signal with the reference level signal and generating the sliced signal according to the result of comparison". However, the device 4 shown in Fig. 1 of Popplewell is an analog to digital converter ... Popplewell fails to read on the comparing device of the applicant's disclosure and fails to teach or suggest the limitation of "comparing the input signal with the reference level signal and generating the sliced signal according to the result of comparison" in claim 1 of applicant's disclosure."

6. Examiner disagrees with Applicant's opinion as, firstly the disclosure of the present invention describes that a comparing device can be analog to digital converter in paragraph 0023, under the heading Detailed Description, that is similar to the cited

prior art reference analog to digital converter, secondly the purpose of the ADC is to generated a digital signal or sliced signal from the analog signal based on a reference signal or clock signal or control signal, i.e. same as the Popplewell ADC is doing. Therefore, examiner believes that the cited reference reasonably teach the limitation so the rejection is upheld.

7. Applicant argument that "... the phase-detecting, level-determining device includes the limitations "detecting the phase at which the transition of the sliced signal occurs". However, the phase detector 5 of Popplewell provides a phase error value representative of a calculated difference between the actual phase of the clock signal and a desired phase, to the digital loop filer 6 (column 3, lines 31-34). Also, the digital filer 6 of Popplewell operates on the phase error value to provide a filtered phase error value to a DAC 7A (column 3, lines 35-37) ... Therefore, the combination of these prior art devices fails to disclose the limitation of the phase-detecting, level-determining device in claim 1 of the applicant's disclosure (emphasis' added).

8. Examiner's response: Popplewell teaches a phase-detecting, level-determining device (5, 6 in figure 1 and figure 3) coupled with the comparing device, wherein the phase detecting level determining device is for detecting the phase at which the transition of the sliced signal occurs (column 4, lines 30-48), based on a reference clock, and generating a digital level signal according to the result of detection. The cited reference teaches a phase detecting device 5 in figure 1, which detects the phase and the level of the signal at which phase changes (column 3, lines 44-60), the phase detecting level determining device determines the amplitude or the level of the input

signal at different time instances where the phase changes. Also in order to correct the phase alignment the system is first determining the phase i.e. the point where the signal changes its phase or it changes its level that causes the phase to change in other words when the input signal is within different levels as shown in the reference the phase is detected accordingly. Therefore, the cited reference discloses or suggests the claimed limitations so the rejection is upheld.

9. Applicant argument that "... the phase detector of Chong only can determine whether a rising edge of the system clock precedes a rising edge of the delayed clock and the up/down counter increases or reduces the delay value according to the comparing result, but the combination of these prior art devices fails to teach or suggest "detecting the phase at which the transition of the sliced signal occurs..."

10. Examiner respectfully traverses Applicant's opinion as the phase detector system of the Chong determines the phase at which the transition of the sliced signal occurs (see figure 5 and column 6 lines 42-67), as specified in the Applicant's argument above, determining a rising edge of the system clock precedes a rising edge of the delayed clock is determining the phase of the signal. Therefore, the rejection to the above claims is not withdrawn.

11. Applicant argument that "...Yamamoto discloses a clock recovery circuit, which compares two sample values, selects a small one thereof, and controls the sampling clock signal ...Therefore, Yamamoto only discloses comparing two sampled values and improves the signal sampling but fails to teach or suggest "determine whether a rising edge of the system clock precedes a rising edge of the delayed clock..."

12. Applicant seems to get confused about the present invention and the cited prior art, Examiner just want to bring this to Applicant notice that the original claim 1 or the amended claim 1 doesn't have above limitation "...determine whether a rising edge of the system clock precedes a rising edge of the delayed clock..." which the Applicant is arguing about. This functionality is actually in the disclosure of one of the cited references i.e. Chong.

13. From the above discussion it is clear that the cited prior art references discloses or teaches or suggests all the limitations. Therefore, the rejection based on the prior art of record to claims 1-2 and 10-17 is upheld.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-2, 12-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6,304,071) in view of Yamamoto (US 6,057,730) further in view of Chong et al. (US 7,200,769).

Regarding Claim 1:

Popplewell et al discloses a digital data recovery circuit (column 1, lines 16-22) for converting an input signal into a sliced signal comprising:

a comparing device (4 in figure 1) coupled with the input signal and a reference level signal for comparing the input signal with the reference level signal (column 3, lines 26-30) and generating the sliced signal according to the result of comparison;

a phase-detecting, level-determining device (5, 6 in figure 1) coupled with the comparing device for detecting the phase at which the transition of the sliced signal occurs (column 4, lines 30-48), based on a reference clock, and generating a digital level signal according to the result of detection; and

a digital-to-analog converter (DAC; 7A in figure 1) coupled with the phase-detecting, level-determining device for generating the reference level signal for the comparing device according to the digital level signal.

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the comparing device for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock, and generating a digital level signal according to the result of detection.

However, Chong et al in the same field of endeavor discloses a system where the detection of the phase at which the transition of the sliced signal occurs (column 8, lines 30-40; figure 3) is determined to accurately correct the phase of the signal. Also Yamamoto in same field of endeavor discloses how the amplitude of signal is detected to correct the phase (column 22, lines 1-15; column 3, lines 45-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a phase detector coupled with a level determining means to detect the phase at which the transition of the sliced signal occurs and generating a

digital level signal accordingly in order to compensate for the variations in the radio propagation characteristics which may cause the signal level shifts to make the average level of signal higher or lower result in improper sliced signal.

Regarding Claim 2:

Popplewell et al discloses all of the subject matter as described above and further discloses that the phase-detecting, level-determining device further comprises:

a phase detector (5 in figure 1; figure 3) coupled with the comparing device for detecting the phase of the sliced signal transiting from a first binary value to a second binary value, and the phase of the sliced signal transiting from the second binary value to the first binary value, based on the reference clock (column 4, lines 30-38).

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that a level determiner coupled with the phase detector for generating the digital level signal according to the result of detection.

However, Chong et al in the same field of endeavor discloses a system where the detection of the phase at which the transition of the sliced signal occurs (column 8, lines 30-40; figure 3) is determined to accurately correct the phase of the signal. Also Yamamoto in same field of endeavor discloses how the amplitude of signal is detected to correct the phase (column 22, lines 1-15; column 3, lines 45-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a phase detector coupled with a level determining means to detect the phase at which the transition of the sliced signal occurs and generating a digital level signal accordingly in order to compensate for the variations in the radio

propagation characteristics which may cause the signal level shifts to make the average level of signal higher or lower result in improper sliced signal.

Regarding Claim 12:

Popplewell et al discloses all of the subject matter as described above and further discloses that the comparing device is an one-bit analog-to-digital converter (ADC) generating the sliced signal (4 in figure 1; column 3, lines 20-25) having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal. it is inherent that the ADC used in the system of Popplewell is of the form of a one bit analog to digital converter.

Regarding Claim 13:

Popplewell et al discloses all of the subject matter as described above and further discloses that the comparing device is an ADC (4 in figure 1; abstract) generating the sliced signal (column 4, lines 49-58) with bit values from 1 to N according to the relationship between the input signal and the reference level signal.

Regarding Claim 15:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the DAC is a voltage source for providing a reference level required by the comparing device.

However, Yamamoto in same field of endeavor discloses DAC is a voltage source for providing a reference level required by the comparing device (206, 207 in figure 2; column 3, lines 55-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a DAC as a voltage source for providing a reference level required by the comparing device in order to make the comparison with the incoming signal easier and by performing multifunction saves circuit space.

Regarding Claim 16:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the DAC is a current source for providing a reference level required by the comparing device converted by an external circuit from a current generated by the DAC.

However, Yamamoto in same field of endeavor discloses DAC is a voltage source for providing a reference level required by the comparing device (206, 207 in figure 2; column 3, lines 55-67) so it is obvious that the DAC could be a voltage source or a current source for the purpose of providing the reference signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a DAC as a voltage source for providing a reference level required by the comparing device in order to make the comparison with the incoming signal easier and by performing multifunction saves circuit space.

Regarding Claim 17:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the DAC is a control circuit for directly controlling the bit value of the sliced signal output by the comparing device.

However, Yamamoto in same field of endeavor discloses DAC is a voltage source for providing a reference level required by the comparing device (206, 207 in figure 2; column 3, lines 55-67) so it is obvious that the DAC could be a voltage source or a current source or a control device for the purpose of providing the reference signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a DAC as a voltage source for providing a reference level required by the comparing device in order to make the comparison with the incoming signal easier and by performing multifunction saves circuit space.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6,304,071) in view of Yamamoto (US 6,057,730) further in view of Chong et al. (US 7,200,769) as applied to claim 1 above, and further in view of Li et al. (US 6,968,026).

Regarding Claim 10:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the phase detector is in a delay locked loop.

However, Li et al in the same field of endeavor discloses a system where the phase detector is in a delay locked loop (column 1, lines 60-67; figure 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a delay locked loop dll to compares the phase of one of its outputs to the input clock to generate an error signal which is then integrated and fed back as the control signal in order to take advantage of dll as it is easy to stabilize and the integration allows the error to go to zero while keeping the control signal, and thus the delays, where they need to be for phase lock.

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6,304,071) in view of Yamamoto (US 6,057,730) further in view of Chong et al. (US 7,200,769) as applied to claim 1 above, and further in view of Matsuda et al. (US 6,519,303).

Regarding Claim 11:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the comparing device is a comparator generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

However, Li et al in the same field of endeavor discloses a system where the comparing device is a comparator (25 in figure 4; column 5, lines 20-30) generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second

binary value when the level of the input signal is higher than the level of the reference level signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a comparator for generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal as it is easier to implement the comparison using a comparator as it can give a signal with different polarity when the incoming signal changes its polarity.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6,304,071) in view of Yamamoto (US 6,057,730) further in view of Chong et al. (US 7,200,769) as applied to claim 1 above, and further in view of Takahashi et al. (US 6,754,018).

Regarding Claim 14:

Popplewell et al discloses all of the subject matter as described above except for specifically teaching that the comparing device is a partial-response maximum likelihood circuit generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

However, Li et al in the same field of endeavor discloses a system where the comparing device is a partial-response maximum likelihood circuit (column 4, lines 5-15) generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a partial-response maximum likelihood circuit for generating the sliced signal having the first binary value when the level of the input signal is lower than the level of the reference level signal and generating the sliced signal having the second binary value when the level of the input signal is higher than the level of the reference level signal.

Allowable Subject Matter

19. Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter: The prior art references Popplewell et al. (US 6,304,071), Yamamoto (US 6,057,730), Chong et al. (US 7,200,769) and Li et al. (US 6,968,026) etc. fails to disclose the phase detector comprises; N flip-flop series wherein each of the flip-flop

series has an input end, a clock input end, and an output end, and each input end of the flip-flop series is coupled with the Kth sliced signal with the clock input end of a flip-flop series being coupled with the signal generated by delaying the reference clock for K/N period; and N transition phase detecting devices wherein each transition phase detecting device has a first input end, a second input end, a first output end, and a second output end; the first input end of an Lth transition phase detecting device is coupled with the output end of the Lth flip-flop series, the second input end of the Lth transition phase detecting device coupled with the output end of an L+ 1th flip-flop series, the first input end of an Nth transition phase detecting device coupled with the output end of an Nth flip-flop series, and the second input end of the Nth transition phase detecting device coupled with the output end of the first flip-flop series, wherein N is a positive integer, K is a positive integer between 1 and N, and L is a positive integer between 1 and N-1.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571)270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./
Examiner, Art Unit 2611
March 24, 2008
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611